REMARKS

Claims 1-20 and 26-27 are pending.

Claims 21-25 were withdrawn in the Request for Continued Examination filed on March 14, 2003 (see Remarks section of that paper).

Claims 1-20 and 26-27 stand rejected.

Claims 10 is amended. No new subject matter is added.

Reconsideration of the pending claims is respectfully requested in light of the following amendments and remarks.

Claim Rejection – 35 USC § 102

Claims 1-27 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,994,732 to Ajika et al. ('Ajika'). Applicants note that claims 21-25 were withdrawn in the Request for Continued Examination filed on March 14, 2003 (see Remarks section of that paper). Claims 1-20 and 26-27 remain rejected under Ajika.

Claim 1 recites, in part, a semiconductor memory device comprising a plurality of sectors on a substrate, each sector comprising memory cell transistors arranged in a cell array block and decoder transistors in a column decoder block, wherein the semiconductor memory device is configured to erase all the memory cell transistors in a sector together.

To the contrary, Ajika FIG. 8 shows that each sector 3a contains a plurality of erase blocks 26, wherein only the memory cell transistors belonging to a single erase block are configured to be collectively erased (column 2, lines 49-52). Thus, Ajika FIG. 8 does not anticipate claim 1 because all the memory cell transistors in a sector are not configured to be erased together.

Claim 10 recites, in part, a nonvolatile semiconductor memory device with a plurality of sectors, each sector comprising a cell array block and a column decoder block. The cell array block further comprises a plurality of word lines, a plurality of bit lines, and a plurality of memory cell transistors having gates and drains, each gate connected to a corresponding word line out of the plurality of word lines, each drain connected to a corresponding bit line out of the plurality of bit lines.

The Examiner has stated that Ajika's region 3a, FIG. 8 is a "sector" and Ajika's erase block 26, FIG. 8 is a "cell array block." Contrary to claim 10, Ajika's erase block does not comprise a plurality of bit lines, rather there is only one main bit line 24 that is connected to the select gate transistors that are located on either side of the erase block (FIGS. 2 and 3; column 7, lines 15-20). Ajika discloses that sub bit lines 19a, 19b are connected to the drains

4 of each memory transistor 11 (FIG. 2 and 3; column 6, lines 63-65), but if the sub bit lines 19a, 19b are considered to be the recited plurality of bit lines then the drains of each of the memory cell transistors are not connected to a corresponding bit line (singular) out of the plurality of bit lines.

Claim 10 also recites that the column decoder block further comprises a plurality of column decoder transistors, each column decoder transistor connected between a corresponding bit line out of the plurality of bit lines and a common data line configured to select one bit line out of the plurality of bit lines.

The Examiner has stated that the select gate transistors 12 within the memory erase blocks 26 are the recited "column decoder block." In this case, the select gate transistors are provided at both ends of the p-well region 3, to either side of an erase block 26 (FIGS. 2 and 3; column 6, lines 52-67).

Pending claims must be given their broadest reasonable interpretation that is consistent with the specification (MPEP 2111). The applicants submit that the Examiner's interpretation of a "column decoder block" is unreasonably inconsistent with the specification, where a "column decoder block" is shown in FIG. 3 as a singular, contiguous area 103, and not as plural areas separated by the erase block 26 as shown in Ajika FIG. 2 and 3. In other words, the applicants claimed a single "column decoder block" having a plurality of column decoder transistors, and not multiple "column decoder blocks" that each have a single select gate transistor.

Furthermore, even if the two select gate transistors shown at either side of the erase block in Ajika FIG. 2 and 3 could be considered a "column decoder block," each of Ajika's select gate transistors is not connected between a corresponding bit line out of the plurality of bit lines as required by claim 10. Rather, both of Ajika's sub bit lines 19a, 19b are connected to one n-type impurity region 15b of the select gate transistor via a contact hole 17 (column 6, lines 65-67), while the other n-type impurity region 15a of the select gate transistor is connected to the main bit line 24 through a contact hole 16 (column 7, lines 17-20). In other words, only one main bit line 24 is connected to the select gate transistors in Ajika's "column decoder block", not a plurality of bit lines. If the sub bit lines 19a, 19b are considered to be the plurality of bit lines, then a corresponding one of them is not connected to each of the select gate transistors in the column decoder block.

For at least the reasons discussed above, Ajika does not anticipate claim 10.

Claim 15 recites, in part a nonvolatile semiconductor memory device comprising a plurality of sector units, each sector unit comprising a common bulk region, wherein each sector unit is configured to be electrically erasable in response to an erase signal.

The Examiner has stated that Ajika's region 3a, FIG. 8 is a "sector" and Ajika's erase block 26, FIG. 8 is a "cell array block." Contrary to claim 15, Ajika explains that only the memory cell transistors belonging to a single erase block 26 in each p-well region 3a are configured to be collectively erased (column 2, lines 49-52). Thus, Ajika FIG. 8 does not anticipate claim 15 because the entire sector unit (composed of a plurality of erase blocks 26) is not configured to be electrically erasable in response to an erase signal. Claim 15 is not anticipated by Ajika for at least this reason.

With respect to claim 18, Ajika FIG. 8 simply does not disclose the limitations of a cell array block arranged in an (M x N) array with M and N both at least equal to two and a column decoder arranged in a (P x N) array with P at least equal to one. The applicants submit that claim 18 is not anticipated by Ajika for at least these reasons.

All the remaining pending claims that have not yet been discussed are dependent upon claims 1, 10, 15, and 18. For at least the above reasons, the applicants submit that the dependent claims are also not anticipated by Ajika.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-20 and 26-27 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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